REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. The independent claims have been amended to more clearly define the present invention over the cited prior art references. Support for the claim amendments may be found in paragraphs 10 and 12 of the specification, for example. Since "gathering" has been removed from the claims, it is submitted that the 35 U.S.C. §112 claim informalities are overcome. The claim amendments and arguments supporting patentablity of the claims are provided below.

I. The Amended Claims

The present invention, as recited in amended independent Claim 1, for example, is directed to a microprocessor comprising a processing unit, a memory connected to the processing unit and comprising an addressable memory space for a lower memory area and an extended memory area, means for connecting to and accessing the addressable memory space, and means for executing instructions of an instruction set executable by the processing unit. The instruction set comprises instructions for accessing the addressable memory space, a first instruction group comprising instructions for accessing the lower memory area, and a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing the extended memory area. The microprocessor also comprises means for preventing access to the extended memory area when executing an instruction in the first instruction group.

Independent device Claim 11 has been amended similar to amended independent device Claim 1, but without some of the means language. Independent method Claim 21 has been amended similar to amended independent device Claim 11.

II. The Claims Are Patentable

The Examiner rejected independent Claims 1, 11 and 21 over the Baum et al. patent. The Baum et al. patent is directed to extended addressing for small addresses obtained for instructions, for operands, and for some control tables in central processor and I/O programs to enable the small addresses to operate with a very large memory. The Baum et al. patent also provides a way to control how the extended addresses are mapped into the same or different sections of the memory.

The Examiner essentially references column 3, line 67 to column 4, line 5 and column 7, lines 12-21 in the Baum et al. patent as disclosing the claimed invention. The Examiner has taken the position that since Baum et al. discloses restricting small-addressed data to the first section of the memory that contains the instructions for generating the small addresses, and the small-addressed data within a given virtual address space can be located in any section of the memory, which may be different from the first section containing the instructions, this corresponds to the first and second instruction groups as recited in the claimed invention.

However, the Baum et al. patent fails to disclose a processor having an instructions set of executable

instructions divided into two groups, namely a first group of instructions for accessing the lower memory area, and a second group of instructions only comprising all of the instructions for accessing the extended memory area. The Examiner referenced column 3, line 64 through column 4, line 5 in the Baum et al. patent as disclosing the first and second group of instructions:

> "In the DAT-ON mode, the invention enables varying degrees of flexibility in section selection for mapping the page frames containing the translated addresses in the very large memory. The flexibility allows all translated addresses of a specific address space to be mapped only in the first section, or in a single section anywhere, or in plural sections including from two sections up to all sections of the very large memory."

In fact, the Baum et al. patent corresponds to the prior art disclosed in the present application concerning microprocessors having a page register for storing the address of a section to be accessed, with the content of this register being concatenated with addresses of conventional size. This approach leads to a division of the addressable space into relatively isolated sections, which imposes additional constraints on the compilers.

In sharp contrast, the claimed invention has been amended to recite that the first instruction group comprises instructions for accessing the lower memory area, and the second instruction group is distinct from the first instruction group and only comprises all of the instructions

for accessing the extended memory area. In addition, access to the extended memory area is prevented when executing an instruction in the first instruction group. In the Baum et al. patent, a processor having an instructions set of executable instructions divided into two groups is not disclosed. Instead, Baum et al. discloses that specific address spaces can be "mapped only in the first section, or in a single section anywhere, or in plural sections" - and no mention is made of a second instruction group being distinct from a first instruction group and only comprising all of the instructions for accessing a particular memory area.

Accordingly, it is submitted that amended independent Claim 1 is patentable over the Baum et al. patent. Amended independent Claims 11 and 21 are similar to amended independent Claim 1. Therefore, it is submitted that these claims are also patentable over the Baum et al. patent.

In view of the patentability of amended independent Claims 1, 11 and 21, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need

to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330